UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/898,699	07/02/2001	Dong-woo Lee	9898-176	2435

20575 7590 08/28/2007	EXAMINER
MARGER JOHNSON & MCCOLLOM, P.C. 210 SW MORRISON STREET, SUITE 400 PORTLAND, OR 97204	HSU, JONI

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

	Application No.	Applicant(s)
Office Action Summary	09/898,699	LEE ET AL.
	Examiner	Art Unit	
	Joni Hsu	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>25 June 2007</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-12,14,15,17,18,20 and 24-31* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-12,14,15,17,18,20 and 24-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All   b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments filed June 25, 2007 have been considered but are not persuasive.

2.   Applicant argues that write port data 202 of Deering (US005544306A) is not external

depth data that was received from the memory controller 70 (pages 8-9).

In reply, the Examiner points out unidirectional connecting lines 202 and 204 of Deering

can be modified so connecting line 202 is combined with connecting line 204 to form a single

bidirectional line connecting compare circuit 235 to memory cell array 56, and so the external

depth data can be transferred via this bidirectional line into the memory cell array 56. It would

have been obvious to modify the device of Deering so that the connecting line is bidirectional so

that external depth data is transferred via the connecting line into the memory cell array.

Deering discloses several bidirectional lines, such as line 60 shown in Figure 2 (c. 8, ll. 34-37).

Bidirectional lines have the advantage of being able to transfer data in both directions on the

same line, therefore conserving circuit space. Bidirectional lines are well-known in the art.

Claim Rejections - 35 USC § 103

3.   The text of those sections of Title 35, U.S. Code 103(a) not included in this action can be

found in a prior Office action.

4.   Claims 1 and 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Deering (US005544306A).

5.   As per Claim 1, Deering teaches memory device (71, Fig. 1) for use with memory

controller (70; c. 5, ll. 66-c. 6, ll. 1), memory device comprising memory cell array (56, Fig. 2; c.

7, ll. 27-30) adapted to store internal depth data of object (c. 8, ll. 30-34; c. 15, ll. 56-61; c. 16, ll.

60-62); compare circuit (235, Fig. 8; c. 15, ll. 56-61); line (204, Fig. 2) connecting the compare

circuit to memory cell array (c. 15, ll. 24-26, 46-49); and data modifying circuit (58) distinct

from memory controller, data modifying circuit including compare circuit (c. 15, ll. 11-13) and

being adapted to receive corresponding new external depth data of the object from the memory

controller (c. 15, ll. 56-61; c. 16, ll. 62-67; c. 5, ll. 66-c. 6, ll. 1), compare the new external depth

data with the internal depth data (c. 15, ll. 56-61), and transfer the external depth data, into the

memory cell array, depending on the result of the comparison, if the external depth data is

transferred, over-write the internal depth data in the memory cell array with the transferred

external depth data, and output to the memory controller a status signal (c. 17, ll. 1-10; c. 5, ll.

66-c. 6, ll. 4; c. 6, ll. 53-62). Deering discloses two lines (202, 204) connecting the data

modifying circuit 58 to the memory cell array 56 for transferring depth data. One connecting

line transfers depth data from the memory cell array 56 to the data modifying circuit 58, which is

connecting line 204 (c. 8, ll. 1-5, 12-14; c. 15, ll. 24-26, 46-49). The compare circuit 235 enables

the other connecting line to transfer external depth data from the data modifying circuit to 58 the

memory cell array 56, which is connecting line 202 (c. 8, ll. 65-67; c. 17, ll. 1-10). Connecting

line 204 is for transferring depth data from the memory cell array 56 to the compare circuit 235

(c. 15, ll. 24-26, 46-49). However, Deering does not explicitly teach transferring the external

depth data, via a line connecting the compare circuit to the memory cell array, into the memory

cell array. However, unidirectional connecting lines 202 and 204 can be modified so that

connecting line 202 is combined with connecting line 204 to form a single bidirectional line

connecting the compare circuit 235 to the memory cell array 56, and therefore the external depth

data can be transferred via this bidirectional line into the memory cell array 56.

It would have been obvious to one of ordinary skill in the art at the time of invention by

applicant to modify the device of Deering so that the connecting line is bidirectional so that

external depth data is transferred via the connecting line into the memory cell array. Deering

discloses several bidirectional lines, such as line 60 shown in Fig. 2 (c. 8, ll. 34-37).

Bidirectional lines have the advantage of being able to transfer data in both directions on the

same line, therefore conserving circuit space. Bidirectional lines are well-known in the art.

6.   As per Claim 24, Deering describes a first control pin (PA_PASS_IN, PA_PASS_OUT,

178, Fig. 8) that directly connects the compare circuit (235) to the memory controller (70, Fig. 1;

c. 16, ll. 39-42; c. 17, ll. 1-10; c. 5, ll. 66-c. 6, ll. 4, c. 6, ll. 53-62), as shown in Fig. 8. Deering

discloses that the FBRAM chip 71 provides one set of pixel port control input/output interface

pins 114 for accessing the pixel buffer 56 via the compare circuit 58 (c. 9, ll. 51-57). Therefore,

Deering discloses that 114 refers to pixel port control input/output interface pins, and since all

control lines go through 114, this means that the control pins 114 directly connect the compare

circuit 58 to the memory controller 70.

7.   As per Claim 25, Deering describes that the first control pin is adapted to receive a first

control signal (PA_PASS_IN) from the memory controller (70, Fig. 1) and to output a first status

signal (PA_PASS_OUT) to the memory controller (c. 17, ll. 1-10; c. 5, ll. 66-c. 6, ll. 4, c. 6, ll.

53-62), as shown in Fig. 8. Deering discloses that the FBRAM chip 71 provides one set of pixel

port control input/output interface pins 114 for accessing the pixel buffer 56 via the compare

circuit 58 (c. 9, ll. 51-57). Therefore, Deering discloses that 114 refers to pixel port control

input/output interface pins, and since all control lines go through 114, this means that the control

pins 114 directly connect the compare circuit 58 to the memory controller 70.

8.   As per Claim 26, Deering describes a second control pin that directly connects the

compare circuit (58, Fig. 4; c. 8, ll. 30-34) to the memory controller (70, Fig. 1; c. 6, ll. 53-62; c.

11, ll. 8-15), as shown in Fig. 4. Deering discloses that the FBRAM chip 71 provides one set of

pixel port control input/output interface pins 114 for accessing the pixel buffer 56 via the

compare circuit 58 (c. 9, ll. 51-57). Therefore, Deering discloses that 114 refers to pixel port

control input/output interface pins, and since all control lines go through 114, this means that the

control pins 114 directly connect the compare circuit 58 to the memory controller 70.

9.   As per Claim 27, Deering describes that the second control pin is adapted to receive a

second control signal from the memory controller (70, Fig. 1) and to output a second status

signal to the memory controller (c. 6, ll. 53-62; c. 11, ll. 8-15), as shown in Fig. 4.

10.   As per Claim 28, Claim 28 is similar in scope to Claim 1, except Claim 28 has the

additional limitation that the data modifying circuit receives the corresponding new external

depth data of the object from the memory controller via a control circuit that is responsive to a

control signal directly from the compare circuit. Deering discloses that the data modifying

circuit (58, Fig. 2) receives the corresponding new external depth data of the object from the

memory controller (70, Fig. 1) (c. 15, ll. 56-61; c. 16, ll. 62-67; c. 5, ll. 66-c. 6, ll. 1). A control

circuit (114, Fig. 4) is connected to the memory controller through bus 64, as shown in Fig. 4 (c.

5, ll. 66-c. 6, ll. 4; c. 15, ll. 56-61; c. 16, ll. 62-67). The data modifying circuit receives the depth

data from the memory controller through the control circuit (c. 16, ll. 39-53). The control circuit

is responsive to a control signal directly from the compare circuit (PA_PASS_OUT 178, Fig. 8

and 9; c. 15, ll. 58-61). Therefore, Claim 28 is rejected under the same rationale as Claim 1.

11.   Claims 3, 5-12, 14, 15, 17, 18, 20, and 29-31 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Deering (US005544306A) in view of Dowdell (US005301263A).

12.   As per Claims 3 and 29, Deering is relied upon for the teachings as discussed relative to

Claim 1. Deering discloses a first control pin for receiving a first control signal from the

memory controller (70, Fig. 1; PA_PASS_IN signal, c. 15, ll. 56-61; c. 17, ll. 2-10; c. 5, ll. 66-c.

6, ll. 4; c. 6, ll. 53-62), as shown in Fig. 10; and a control circuit for transmitting the external

depth data to the memory cell array (56, Fig. 2; c. 8, ll. 30-34; c. 15, ll. 56-61; c. 16, ll. 62-67).

       However, Deering does not teach bypassing data modifying circuit depending upon state

of first control signal (81E, Fig. 9). The specification describes bypassing data modifying circuit

depending as an instant where depth compare writing is not going to occur (Specification p. 5, ll.

9-21). Dowdell teaches similar process as follows in that incoming z-buffer address, new z-

value are given as entry into FIFO 102. Controller 112 has to act on incoming pixel address to

update the new z-value, if necessary. Dowdell makes use of an INVALID bit to validate a new

z-value to be written to memory (Col. 4, lines 3-67). The most significant, middle significant,

and least significant bytes of the old 24 bit z-values, R1, R2 and R3 and corresponding bytes of

the new 24 bit z-value denoted by W1, W2 and W3 and a comparison is performed between R1

and W1 and if R1>W1, as determined by the comparator 114, Figure 2, then it is determined the

entire 24 bit old z-value is greater than the entire 24 bit new z-value and consequently the entire

24 bit new z-value consisting of W1, W2 and W3 must be written to memory 124; however, if

R1<= W1, then the old 24 bit z-value is less than the new 24 bit z-value, indicating that the new

value should not be written to memory and in this case, the updating operation is terminated

immediately. Other comparisons between R2-W2; R3-W3 are detailed and termination of

updating operation is detailed based on the comparisons (c. 4, ll. 45-67; c. 5, ll. 1-55). Thus

INVALID bit state is the signal which then determines bypassing of the update operations.

It would have been obvious to one of ordinary skill in the art at the time of invention by

applicant to modify the device of Deering to include bypassing the data modifying circuit

depending upon a state of the first control signal as suggested by Dowdell because it results in

conserving computing resources as no comparison has to take place.

13.   As per Claims 5, 18, and 20, Deering discloses that the status signal is output through the

first control pin (c. 17, ll. 3-5), as shown in Fig. 10.

14.   As per Claims 6, 7, 14, 30, and 31, Deering does not teach a register explicitly for the

purpose of storing the received new external depth data. However, Dowdell's invention

discloses in Figure 1 a three-step updating operation (i.e., read, compare, write) for a given pixel

and a compare circuit (equal comparator 112, greater than comparator 114, Fig. 1, Dowdell).

It would have been obvious to one of ordinary skill in the art at the time of invention by

applicant to modify the device of Deering to include a register explicitly for the purpose of

storing the received new external depth data as suggested by Dowdell because it provides for

efficient data processing as z values are updated only if they are determined to be updated and

unnecessary processing steps are eliminated resulting in processing efficiencies.

15.   As per Claim 8, Deering teaches compare circuit (235, Fig. 8; c. 16, ll. 48-42) adapted to

output status signal to memory controller (70; c. 17, ll. 1-5; c. 5, ll. 66-c. 6, ll. 4; c. 6, ll. 53-62).

16.   As per Claims 9-11, Deering is silent about wherein compare circuit compares internal

depth data with stored external depth in units of X bits/NX bits when second control signal is in a

non-active/active state. However, Dowdell teaches making use of an INVALID bit that indicates

for a particular pixel whether or not the corresponding z-value memory location has a valid z-value stored in it, with a value of '0' indicating that it does and a value of '1' indicating that it does not. Further, Dowdell discloses most significant, middle significant and least significant bytes of old z-value and new z-value being compared, and this it does not by processing all bits at once. Figure the MSB are compared, then middle significant and then least significant bytes and avoids unnecessary processing using this logic (c. 4, ll. 40-67; c. 5, ll. 1-55) and INVALID bit (c. 4, ll. 3-10), providing a valid status for a z-value at a particular memory location.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Deering so that the compare circuit compares the internal depth data with the stored external depth in units of X bits/NX bits when the second control signal is in a non-active/active state as suggested by Dowdell because it results in efficient processing of z-values in the comparator circuit.

17.   As per Claim 12 and 17, Deering describes a method of processing depth data of an object (c. 8, ll. 32-34) in a memory device (71, Fig. 1) controlled by a memory controller (70; c. 5, ll. 66-c. 6, ll. 1), the method comprising receiving external depth data of the object from the memory controller (c. 15, ll. 56-61; c. 16, ll. 62-66; c. 5, ll. 66-c. 6, ll. 1); storing the received external depth data (c. 8, ll. 30-34); receiving a first control signal from the memory controller through a first control pin distinct from the memory controller (PA_PASS_IN, c. 15, ll. 56-61; c. 17, ll. 3-7; c. 5, ll. 66-c. 6, ll. 4; c. 6, ll. 53-62), as shown in Fig. 10; receiving the stored external depth data and corresponding internal depth data stored in the memory cell array (56, Fig. 2) at a compare circuit (235, Fig. 8; c. 15, ll. 11-13; c. 15, ll. 56-61; c. 16, ll. 60-62) that is distinct from the memory controller and connected via a line (204, Fig. 2) to the memory cell array (c. 15, ll.

24-26, 46-49) comparing, the received data, writing from the compare circuit, the external depth

data over the corresponding internal depth data in the memory cell array depending on the result

of the comparison (c. 17, ll. 1-10); and receiving a second control signal from the memory

controller through a second control pin distinct from the memory controller (c. 6, ll. 53-62), as

shown in Fig. 4. Deering discloses two lines (202, 204) connecting the data modifying circuit 58

to the memory cell array 56 for transferring depth data. One connecting line transfers depth data

from the memory cell array 56 to the data modifying circuit 58, which is connecting line 204 (c.

8, ll. 1-5, 12-14; c. 15, ll. 24-26, 46-49). The compare circuit 235 enables the other connecting

line to transfer external depth data from the data modifying circuit to 58 the memory cell array

56, which is connecting line 202 (c. 8, ll. 65-67; c. 17, ll. 1-10). Connecting line 204 is for

transferring depth data from the memory cell array 56 to the compare circuit 235 (c. 15, ll. 24-26,

46-49). However, Deering does not explicitly teach transferring the external depth data, via a

line connecting the compare circuit to the memory cell array, into the memory cell array.

However, unidirectional connecting lines 202 and 204 can be modified so that connecting line

202 is combined with connecting line 204 to form a single bidirectional line connecting the

compare circuit 235 to the memory cell array 56, and therefore the external depth data can be

transferred via this bidirectional line into the memory cell array 56. This would be obvious for

the same reasons given in the rejection for Claim 1.

However, Deering does not disclose determining state of control signal whether active or

inactive and comparing the internal/external depth data in units of X/NX bits; and outputting a

status signal indicating that the NX bits of the internal depth have been modified. However,

Dowdell teaches an INVALID bit which is similar to the control signal with active or inactive

states, in that INVALID bit for a particular pixel indicates whether or not the corresponding z-value memory location has a valid z-values stored in it. Dowdell does the 24 bit bits processing for comparing not at once, instead it does so based on MSB-LSB comparison thus avoiding unnecessary comparison steps (c. 4, ll. 5-67; c. 5, ll. 1-55). Dowdell does the reporting of comparison bits and their modification, if carried out, as indicated by "done" state of Fig. 2.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Deering to include determining a state of the control signal whether active or inactive and comparing the internal/external depth data in units of X/NX bits; and outputting a status signal indicating that the NX bits of the internal depth have been modified as suggested by Dowdell because it provides a more efficient z-value comparison logic.

18.   As per Claim 15, Deering does not teach that writing the external depth data takes place if the comparison yields that the external depth data is larger than the internal depth data. However, Dowdell discloses bytes R1, R2, and R3 of the old z-values and W1, W2, and W3 of the new z-values (c. 4, ll. 45-50) and a comparison is performed between R1 and W1 and if R1>W1, then it is determined that the old z-value is greater than the new z-value and consequently the new z-value is written to memory 124 (c. 5, ll. 5-10). This would be obvious for the same reasons given in the rejection for Claim 3.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing

date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The

examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

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may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

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